ABSTRACT OF THE DISCLOSURE

A memory circuit generally comprising a bit cell, a sense amplifier, and a control circuit. The bit cell may be configured to generate a bit signal. The sense amplifier may be configured to generate a reset signal in response to sensing the bit signal. The control circuit may be configured to (i) set a control latch in response to a detection signal and (ii) reset the control latch in response to the reset signal, wherein the control latch is set while both the detection signal and the reset signal are in an asserted state.